

ABSTRACT OF THE DISCLOSURE

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In a variable gain digital filter of the prior art in which X is the number of bits of data after baseband processing and Y is the number of gain bits, the number of bits of input is $X + Y$ and the number of flip-flops required is equivalent for $(X + Y) \times n$ bits, thereby raising the problem of excessive circuit scale. In the A variable-gain digital filter of the present invention, includes a selector and multiplier for regulating gain are arranged inside the digital filter for regulating gain whereby the number of bits of filter input is X , the number of flip-flops inside the filter is $X \times n$ bits, and a $(Y \times n$ bit) reduction in the number of flip-flops is enabled. The gain regulation circuit that was arranged to precede the prior art filter is thus incorporated within the digital filter to enable enables a reduction in circuit scale.